

Appl. No. 09/971,097

Amdt. Dated 8/4/2005

Response to Office Action Dated 05/10/2005

REMARKS

Claims 1-74 are pending. No new matter has been added.

In conjunction with the undersigned taking responsibility for this Application, considerable effort has been made to overcome pre-existing informalities and shortcomings. Unfortunately, this results in some extra effort for the Examiner. The undersigned wishes to apologize for this, and has endeavored to attend to all details and relieve the Examiner of burdens whenever possible.

Disclaimers Relating to Claim Interpretation and Prosecution History Estoppel

Claims 1-10 have been amended notwithstanding the belief that these claims were allowable. Except as specifically admitted below, no claim elements have been narrowed. Rather, cosmetic amendments have been made to the claims and to broaden them in view of the cited art. Claims 1-10 have been amended solely for the purpose of expediting the patent application process, and the amendments were not necessary for patentability.

Any reference herein to "the invention" is intended to refer to the specific claim or claims being addressed herein. The claims of this Application are intended to stand on their own and are not to be read in light of the prosecution history of any related or unrelated patent or patent application. Furthermore, no arguments in any prosecution history relate to any claim in this Application, except for arguments specifically directed to the claim.

Drawings

The Draftsman did not object to any of the drawings. Formal drawings have been submitted along with this response.

Information Disclosure Statements

One Information Disclosure Statement has been filed in this Application. Consideration of this IDS is respectfully requested.

27/37

Appl. No. 09/971,097

Amdt. Dated 8/4/2005

Response to Office Action Dated 05/10/2005

Specification

The Examiner objected to the following informalities.

The Examiner objected to "source ports 10 numbered 0 through 64" on page 3 line 14, published in paragraph 0020 lines 2-3. The Examiner suggested replacing these lines with "source ports 11 numbered 0 through 63." Instead, page 3 line 14 was amended to recite --source ports 10 numbered 0 through 63--. In addition, Fig. 3 was amended to label source ports 0 through 63 as --ports 10-- to correlate the cross-reference.

The Examiner objected to "ports 10" on page 3 line 15, published in paragraph 0020 line 5. The Examiner suggested replacing "ports 10" with "ports 11" because Fig. 3 shows "ports 11." Instead, as above, Fig. 3 was amended to label source ports 0 through 63 as --ports 10-- for consistency with Fig. 5, which also shows "ports 10." Thus, page 3 line 15 was not amended.

Therefore, the above objections should be withdrawn.

Claim Objections

The Examiner objected to claims 1-10. These objections are respectfully traversed. The Examiner pointed to the following informalities:

In claim 1 line 6, the Examiner suggested replacing "a said ingress source port" with --said ingress source port-- to correct a typographical error. In claim 1 line 10, published in claim 1 line 15, the Examiner suggested replacing "said input source port" with --said ingress source port-- for consistency. It is believed that claim 1, as amended, no longer has informalities as indicated by the Examiner.

In claim 2 line 6, the Examiner suggested replacing "a said ingress source port" with --one of said ingress source ports--. In claim 2 line 7, the Examiner suggested replacing "said data packet" with --each of said data packets--. In claim 2 line 9, the Examiner suggested replacing "a said source

Appl. No. 09/971,097

Amdt. Dated 8/4/2005

Response to Office Action Dated 05/10/2005

port" with --one of said ingress source ports--. It is believed that claim 2, as amended, no longer has informalities as indicated by the Examiner.

Finally, the Examiner objected to claims 3-10 because they depend upon objected claim 1. Claim 1 has been amended and overcomes the Examiner's objections.

Thus, the above objections should be withdrawn.

Claim Rejections - 35 USC § 112

The Examiner rejected claims 1-10 under 35 USC § 112, second paragraph as indefinite. This rejection is respectfully traversed.

The Examiner noted that "said input source port" and "said source outputs" in claim 1 lines 10, 13 lacked clear antecedent basis because no input source port and no source outputs had been previously recited in the claim.

Claim 1 line 10 has been amended to replace "said input source port" with --at least one of the source ports--. This amendment provides consistency with "a plurality of source ports" recited in claim 1 line 3. Moreover, "a plurality of source ports" now provides antecedent basis for the amended term.

Additionally, claim 1 line 13 has been amended to replace "said source outputs" with --the source port outputs--. This amendment provides consistency with "a plurality of source port outputs" recited in claim 1 line 7. Moreover, "a plurality of source port outputs" now provides antecedent basis for the amended term.

The Examiner further noted that the phrase "the next available SE" in claim 2 lines 10-11 lacked clear antecedent basis. Claim 2 lines 10-11 have been amended to recite --a next available switching element--. As such, claim 2 now recites "determining a next available switching element by monitoring a last used switching element."

Appl. No. 09/971,097

Amdt. Dated 8/4/2005

Response to Office Action Dated 05/10/2005

Finally, the Examiner noted that the phrase "said switching means" in claim 5 line 2 lacked clear antecedent basis. Claim 5 line 2 has been amended to recite --the apparatus is operable to respond--, thereby eliminating the term lacking antecedent basis.

Thus, the Examiner's rejections should be withdrawn. In addition, cosmetic amendments have been made to claims 1-10. These amendments were not necessary for compliance with 35 USC § 112.

Claim Rejections - 35 USC § 102

The Examiner rejected claims 1-10 under 35 U.S.C. § 102(b) as anticipated by Fischer et al. (USP 5,317,561). This rejection is respectfully traversed.

Fischer et al. disclose a method for switching message cells of a message cell stream according to an asynchronous transfer mode (ATM), including an HTU adaptor, DMUX distributor, multiple switching networks consisting of modules that further contain switching elements, a MUX combiner, and a RES output. In Fischer et al., data is routed to one of two paths, depending on the data rate of the message cell stream. For data rates that do not exceed an individual switching network input, data is supplied to an HTU adaptor via IL1, and distributed to a single switching network input. For data rates that exceed an individual switching network input, data is supplied to an HTU adaptor via IL2, and supplied to a distributor (DMUX) that distributes the data to multiple switching network inputs. Within each switching network, the data is routed according to a three-stage, non-convoluted structure formed by a plurality of modules. The routed data is then supplied to a combiner (MUX) and subsequently, a RES for transmission.

Fischer et al. suggest that a person of ordinary skill in the art may provide a plurality of switching network inputs such that the sum of the transmission bit rates of the switching network inputs at least corresponds to the transport bit rate of the message cell stream. However, Fischer et al. do not disclose, teach or suggest that this functionality can be accomplished by anything other than a switching network structure, consisting of modules and further consisting of switching elements. It is

Appl. No. 09/971,097

Amdt. Dated 8/4/2005

Response to Office Action Dated 05/10/2005

indeed apparent that in Fischer et al., this modular structure is necessary to allow "a message cell supplied to an input of a switching network matrix" to be "through-connected to a specific output of the switching network level via different modules."¹

Fischer et al. further suggest that "the switching elements of the module are interconnected" such that "every input line of the module can be through-connected to every output line of the module."² However, Fischer et al. disclose a structure with two separate input trunks wherein data at speeds lower than the switching network operating speed is supplied to a first trunk IL1 and data at speeds higher than the switching network operating speed is supplied to a second trunk IL2. According to Fischer et al., moreover, the message cells of a message cell stream" can be "distributed pseudo-randomly over all modules of the second stage of the switching network"³ Thus, in Fischer et al., it appears that the physical routing path is dependent upon the data rate of the incoming message cell stream and the path through the convoluted structure of the switching network matrix.

Fischer et al. further suggest that the message cells may be "cyclically distributed over the switching network inputs" such that the message cell stream yields a "uniform distribution of message cells."⁴ However, the apparatus in Fischer et al. limits the operation of the disclosed distributor. When distribution of message cells is undertaken by a single distributor for all switching network matrices, an outage of a single module on one of the switching networks requires a bypass of "the corresponding module of the redundant switching network matrix" in the "further through-connection of message cells."⁵ When distribution is undertaken by one distributor per switching network matrix, "the distribution of message cells can occur independently of the respective structure of the redundant switching network matrices."⁶ Therefore, in Fischer et al., the inner structure of

1 Fischer et al. 3:32-35.

2 Fischer et al. 3: 45-46.

3 Fischer et al. 6:9-11.

4 Fischer et al. 2:14-17.

5 Fischer et al. 6:17-23.

6 Fischer et al. 6:28-33.

Appl. No. 09/971,097

Amdt. Dated 8/4/2005

Response to Office Action Dated 05/10/2005

multiple switching networks necessarily requires a corresponding number of dedicated distributors, necessitating a complex apparatus in order to increase the maximum efficiency of each switching element.

Claim 1 is directed to a high data rate switching apparatus. It recites “a plurality of source ports . . . wherein the effective data rate from the source port outputs to the switching element inputs and from the switching element outputs to the destination port inputs is the higher data rate and the complete data packets of variable or fixed size are transferred through a single serial link.” The single serial link is “formed by a given one of the source ports, a given one of the switching elements and a given one of the destination ports,” and is connected by “a plurality of switching element inputs individually connected to each of the source port outputs” and “a plurality of destination port inputs individually connected to each of the switching element outputs.”

Fischer et al. do not disclose, teach or suggest “a plurality of source ports . . . wherein the effective data rate from the source port outputs to the switching element inputs and from the switching element outputs to the destination port inputs is the higher data rate and the complete data packets of variable or fixed size are transferred through a single serial link.” Instead, Fischer et al. disclose a modular-based architecture composed of internal SEs as its switching network. As a necessary implication of its modular-based architecture, a given message cell may take any of a number of pseudo-random paths to arrive at a given destination. In contrast, the invention of claim 1 has a predetermined path, “the switching elements and the source ports operating to change a given one of the source port outputs successively from a given one of the switching elements to a next available switching element in response to a data packet event.” Therefore, Fischer et al. do not disclose, teach or suggest an apparatus wherein “a complete data packet of variable or fixed size is transferred through a single serial link.”

Claim 2 is directed to a method for routing data. Claim 2 discloses a method wherein “complete data packets are routed from the plurality of destination ports to a given one of the plurality of source ports on a single serial link while sustaining the effective throughput of data at

Appl. No. 09/971,097

Amdt. Dated 8/4/2005

Response to Office Action Dated 05/10/2005

the higher data rate.” The single serial link is provided by “receiving the complete data packets on a given one of a plurality of switching element inputs that are individually connected to the source port outputs” and by “successively receiving the data packets at the lower data rate on a given one of a plurality of destination port inputs that are individually connected to the switching element outputs in response to the data packet event.”

Fischer et al. do not disclose, teach or suggest a method wherein “complete data packets are routed from the plurality of destination ports to a given one of the plurality of source ports on a single serial link while sustaining the effective throughput of data at the higher data rate.” Fischer et al. instead disclose a method wherein the physical routing path of message cells is dependent upon the data rate of the incoming message cell stream and the path through the convoluted structure of the switching network matrix. In Fischer et al., the physical path for routing message cells within message cell streams that exceed the operating speed of a switching element is different than message cells within message cell streams that do not exceed the operating speed of the switching element. The method of claim 2 is not limited to two physical paths.

Additionally, claim 2 recites a method comprising “successively distributing complete data packets at a lower data rate on a plurality of source port outputs that form multiple parallel channels to a plurality of switching elements in response to a data packet event.” Moreover, claim 2 recites “determining a next available switching element by monitoring a last used switching element or a failed switching element.”

Fischer et al. do not disclose, teach or suggest a method comprising “successively distributing complete data packets at a lower data rate on a plurality of source port outputs that form multiple parallel channels to a plurality of switching elements in response to a data packet event.” Instead, Fischer et al. disclose that the inner structure of multiple switching network matrices require a corresponding number of dedicated distributors. If Fischer et al. provided only a single distributor for multiple switching network matrices, a failure of one switching element on a switching network matrix would prevent a corresponding switching element on another

Appl. No. 09/971,097

Amdt. Dated 8/4/2005

Response to Office Action Dated 05/10/2005

switching network matrix from being used. The method of claim 2 has no such limitation.

Therefore, the rejections of claims 1-10 as anticipated by Fischer et al. should be withdrawn.

Claim Rejections - 35 USC § 103

The Examiner rejected claims 5-6 under 35 U.S.C. § 103(a) as obvious from Fischer et al. (USP 5,317,561) in view of Abu-Amara et al. (USP 6,026,092). In addition, the Examiner rejected claims 9-10 under 35 U.S.C. § 103(a) as obvious from Fischer et al. (USP 5,317,561) in view of Li (USApp 2001/0053157). These rejections are respectfully traversed.

In *Claim Rejections - 35 U.S.C. § 102* above, it was shown that Fischer et al. do not disclose, teach or suggest claim 1. As claims 5-6 and claims 9-10 are dependent upon claim 1, the Examiner's rejections should be withdrawn.

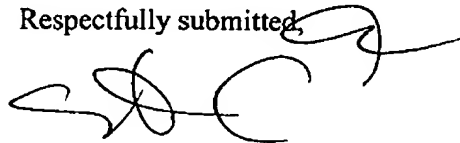
Conclusion

It is submitted, however, that the independent and dependent claims include other significant and substantial recitations which are not disclosed in the cited references. Thus, the claims are also patentable for additional reasons. However, for economy the additional grounds for patentability are not set forth here.

In view of all of the above, it is respectfully submitted that the present application is now in condition for allowance. Reconsideration and reexamination are respectfully requested and allowance at an early date is solicited.

The Examiner is invited to call the undersigned attorney to answer any questions or to discuss steps necessary for placing the application in condition for allowance.

Respectfully submitted,



Steven C. Sereboff, Reg. No. 37,035

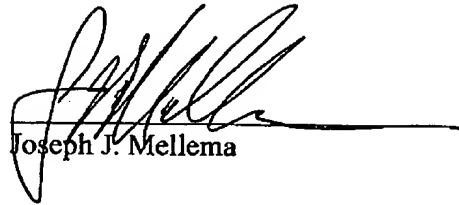
Date: August 4, 2005

34/37

Appl. No. 09/971,097

Amdt. Dated 8/4/2005

Response to Office Action Dated 05/10/2005



Joseph J. Mellema

SoCal IP Law Group LLP
310 N. Westlake Blvd., Suite 120
Westlake Village, CA 91362
Telephone: 805/230-1350
Facsimile: 805/230-1355
email: info@socalip.com

Appl. No. 09/971,097

Amdt. Dated 8/4/2005

Response to Office Action Dated 05/10/2005

Appendix
Marked-Up Versions of Specification and Abstract
Showing Insertions and Deletions

Abstract:

~~Switching apparatus is provided for example for a~~ A ~~high data rate internet switching system using~~
~~switch is disclosed. The switch may include~~ fiber optic channels where ~~the~~ a plurality of switching
elements ~~which are a portion of a switching fabric of the switching apparatus necessarily operate at a~~
significantly lower data rate. ~~Data packets are routed~~ providing routing of variable or fixed size data
packets from a plurality of ingress source ports to a plurality of egress destination ports ~~over~~ via a
single serial link. This is ~~may be~~ provided by ~~the process of~~ storing the high rate data temporarily in
memory in an ~~each of the~~ ingress source ports and then downloading it at a lower rate in a complete
data packet to ~~one~~ a designated ~~switch~~ switching element, ~~and~~ almost immediately ~~switching~~
distributing the next data packet that has been received ~~in~~ by the ingress source port to ~~the~~ a next
switching element. The ~~switch~~ switching element configuration provides ~~an~~ automatic redundancy
~~even if one element fails~~ and a minimum amount of frame overhead while sustaining throughput at
the high data rate.

Specification:

Fig. 3 is an overall diagram of the switching apparatus where there are a number of ~~ingress~~
source ports 10 numbered 0 through 64 63 each receiving from, for example a framer which
normally puts together a digital data packet, at a rate of 10 Gbps. The ~~ingress source~~ ports 10 include
a TM (traffic manager) and a communications processor (CP) and are labeled ~~TM/CP~~ CP/TM. Each
source port has an 8-line output port, each individually coupled to an input port of switch elements
SE0 through SE7 which together create a so-called switching fabric. In turn, the eight ~~switch~~
switching elements each with 64 input ports and 64 output ports are similarly connected on an output
side to ~~egress~~ destination ports 12 also designated CP/TM which have 8-line inputs and are

Appl. No. 09/971,097

Amdt. Dated 8/4/2005

Response to Office Action Dated 05/10/2005

numbered 0 through 63. The combination of the 64 ~~ingress~~ source ports and 64 ~~egress~~ destination ports make up a 64_port ~~full~~ full duplex port.